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Automatic Doppler Control for the West Ford Antenna Pointing System

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

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ABSTRACT

An automatic doppler control system has been added to the West Ford site. This system permits generation of local oscillator frequencies by use of a frequency synthesizer which is in turn driven by the normal West Ford Pointing System, local analog pointing systems, or the Haystack-West Ford intersite coupling system.

Accepted for the Air Force
Franklin C. Hudson, Deputy Chief
Air Force Lincoln Laboratory Office

AUTOMATIC DOPPLER CONTROL FOR THE WEST FORD ANTENNA POINTING SYSTEM

I. GENERAL

The original design concept for the West Ford Antenna Pointing System specified that computed doppler should be displayed on a set of decimal indicators, and that an operator should manually change the local oscillator frequency in accordance with this display. For several reasons, this has proven awkward, and the availability of a frequency synthesizer in early 1964 prompted the decision to automate this part of the system.

II. AUTOMATIC CONTROL SYSTEM

A simplified block diagram of the automatic control system is shown in Fig. 1. The control panel provides switches which enable the operator to select the following modes of operation:

1. Manual. Three BCD thumbwheel switches permit doppler to be varied from + 399 Kc to -340 Kc. (LSB = 1 Kc)
2. Automatic, Analog. The computed doppler from the site's analog computer controls the doppler frequency over the same range.
3. Automatic, Digital. The computed doppler from the local digital paper tape pointing system or from the Haystack-West Ford intersite coupling link controls the doppler frequency over the same range. An additional control panel switch permits the selection of either monostatic or bistatic commands in this mode.

In the manual and digital modes, the doppler command is routed through selection logic to a BCD to binary converter. Additional logic selects either this output or the analog computer command (in the analog mode) and supplies the desired command in serial form to an adder. The other input to the adder comes from a shift register (the arithmetic register) which is preset to a number corresponding to zero doppler. The adder adds the command to (or subtracts it from, according to the command sign) this preset number, and the resulting sum (or difference) is shifted back into the shift register. At the end of the addition process, therefore, the shift register contains the original preset ± the command.

This number is then transferred to the command storage register which is connected to a binary-to-octal converter, and this device provides the proper outputs to drive the frequency synthesizer.

III. FREQUENCY SYNTHESIZER

The frequency synthesizer generates frequencies over the range of 13. 19825 Mc to 14. 222 Mc in 250-cps steps (4096 possible frequencies) in response to a digital input command. The synthesizer is divided into four stages, each of which accepts an octal command. Each stage effectively adds a frequency increment, determined by the stage input command, to the synthesizer's base frequency of 13. 19825 Mc. Table I shows the increments added by each stage for each command.

The West Ford system requires a center frequency (zero doppler) of 13 Mc which is obtained from the synthesizer in the following manner. The preset command is 6527 (octal); the contributions from each stage (according to Table I) are:

Stage	Command	Increment
4	6	768, 000
3	5	80, 000
2	2	4, 000
1	7	1, 750
	Total	853, 750
	Base Frequency	13, 198, 250
	Total	14, 052, 000 cps

The resulting output is doubled (to 28, 104, 000 cps) and then mixed with 15. 104 Mc, giving the final desired output of 13 Mc.

IV. DETAILED SYSTEM DESCRIPTION

A. Control Panel and Monostatic and Bistatic Cabling (Figs. A-1 and A-2)

Figure A-1 shows the mode switches, the manual BCD thumbwheel switches, and the cabling to the selection logic. Figure A-2 shows the cabling for the monostatic and bistatic doppler commands between the West Ford equipment doppler display register and the selection logic.

B. Selection Logic (Fig. A-3)

The diagram shows the logic used to select the Manual, Monostatic and Bistatic inputs. All of the matrices are identical (except for the bottom two sections of

IV. H-4); the top section of each matrix is enabled when the manual mode is selected, and a transfer pulse (20 cps) is gated by the data line from the manual selection switch. Similarly, the middle and lower sections are enabled by the Automatic Digital Monostatic and Automatic Digital Bistatic modes, respectively. These matrix outputs load the command data into the BCD to binary converter (Fig. A-4) via inverters IV. H-2 and IV. H-6.

Of the two lower sections of matrix IV. H-4, the uppermost selects the sign bit from the appropriate source; the bottom section gates a transfer pulse whenever the sign is negative or whenever the Analog mode is selected, and this pulse is used to clear the carry flip-flop (Fig. A-6).

C. BCD-to-Binary Converter (Fig. A-4)

The BCD-to-binary converter accepts a BCD number from the source selection logic and converts it to a binary number.

One well known pencil and paper method for converting a decimal number to its binary equivalent is successive division of the decimal number by two with the remainders of each division forming the binary equivalent. As an example, consider the decimal number 37:

		Remainders
2	37	
2	18	1
2	9	0
2	4	1
2	2	0
2	1	0
	0	1

Reading the remainders from bottom to top, we get 100101 which is the binary equivalent of 37.

The converter uses essentially the same scheme. Division by two is accomplished by shifting to the right at each clock pulse. Consider the units section of the converter (stages DB_7 through DB_{10}): so long as the output of DB_6 is a zero, this section of the converter acts as a normal shift register and its contents are divided by two with every right shift clock. Whenever DB_6 contains a one, however, the rules change,

since this bit has a value of 10, the logic causes the units section to assume the state:

$$\frac{x}{2} + \frac{10}{2}$$

or

$$\frac{x}{2} + 5$$

where x represents the previous state of the section.

The same rule applies to the tens section of the converter (the hundreds section is degenerate in that the input from the next higher digit is always zero) with the result that the BCD number is divided by two with each right shift, and the remainders automatically appear at the output of stage DB_{10}.

The conversion process is illustrated in Fig. A-9 which shows the states through which the converter goes in converting the number 285 from BCD to binary.

D. Arithmetic Register and Command Storage (Fig. A-5)

The arithmetic register is a 16-stage shift register which is preset to:

0000001010101011

by the 20-cps clock.

Consider the underlined groups and imagine an extra "one" at the right-hand end, and another "one" in the most significant bit of the left-most group. This imagined number is octal 6527 which, when used as a command to the frequency synthesizer, results in the zero doppler frequency (13 Mc). The imagined bits are missing because they are not needed in the arithmetic operation, as they are always "ones" over the entire doppler spread.

After this register has been preset, an addition cycles occurs. The add clock consists of a burst of 16 pulses occurring at a 125-Kc rate. This is the same clock used in the AZ/EL arithmetic section of the West Ford machine.

The number from the arithmetic register is shifted to the adder (Fig. A-6) where is is added bit by bit (LSB first) to the command number from the BCD to binary converter (or from the analog computer in the analog mode). The least significant (LSB) bit of the preset number corresponds to 0.5 Kc, and the LSB of the command corresponds to 1 Kc. As a result, the command number is effectively divided by two during the addition process. This is necessary because of the frequency doubling that occurs before the final synthesizer output.

The adder output is shifted back into the preset register so that at the completion of the addition process this register contains the preset number ± the command number. The next 20-cps clock simultaneously presets the register again and transfers the computed command (the preset ± command) to the command storage register. The outputs of this register drive binary-to-octal converters which drive the synthesizer. (Note that the LSB input to the binary-to-octal converter for stage one and the MSB input to the binary-to-octal converter for stage four are wired to fixed logic levels; these are the missing bits in the preset number).

E. Adder (Fig. A-6)

The adder consists of matrix IV. H-10-1 and carry flip-flop IV. H-11-1. Matrix IV. H-10-21 selects either the analog or the digital command, depending on the selected mode of operation and further selects the normal or inverted digital command, depending on the command sign.

Whenever the command sign is plus, the command must be subtracted from the preset number; conversely, when the command sign is minus, the command must be added to the preset number. The adder performs subtraction by adding the complement of the number to be subtracted (the subtrahend — in this case, the command number) to the minuend (the preset number).

The selection of the inverted command in matrix IV. H-10-21 provides the adder with the "ones" complement of the command, but the subtraction process requires a "two's" complement ("two's" complement = "ones" complement + 1). This is provided by presetting the carry flip-flop to the "one" state before the arithmetic cycle occurs whenever a plus sign is encountered in the digital mode (Matrix IV. H-10-30). In all other cases, the carry flip-flop is cleared prior to the arithmetic cycle.

In the analog mode, a shaft encoder is used to provide the command input, and this device automatically supplies "two's" complements for positive signs.

F. Command Inhibit During A-Block Read-In (Fig. A-6)

When an A-block is read in from the paper tape, the doppler display register is cleared at the start of the read-in time and is loaded serially close to the end of read-in time. As a result, this register is empty for almost 0. 25 sec. every time an A-block is read in. In order to prevent the doppler command to the synthesizer from following this transient, it is necessary to inhibit the 20-cps read-in clock to the command register (Fig. A-5) during the A-block read-in time. Fortunately, a

function (FS*) exists which comes true at the beginning of this time and stays true until the new doppler data is loaded.

Assume that an A-block read-in is initiated. This always occurs just after a 20-cps clock, and, therefore, a bona-fide doppler command is transferred to the BCD-to-binary converter by this particular clock. The next 20-cps clock will transfer a zero command to the converter, but it will transfer a bona-fide command from the preset register to the command storage register. This clock is gated by FS*, which is now true, to clear flip-flop IV.H-11-21, thus shutting off matrix IV.H-8-1. Subsequent 20-cps clocks, therefore, cannot load the command storage register, so the last bona-fide command will be preserved.

After the A-block is read in, FS* goes false, and the next 20-cps clock transfers a new bona-fide command to the BCD-to-binary converter and also sets flip-flop IV.H-11-21. Commencing with the next following 20-cps clock, normal operation is restored.

The other sections of matrix IV.H-8 permit normal operation in the manual mode and in the event that the intersite coupling link is being used.

G. Analog Computer Input (Fig. A-7)

The analog computer provides doppler commands by positioning a shaft to which is attached a 13-bit binary encoder. Except for the number of bits, this encoder is identical to those used in the AZ/EL system. A set of contacts in the encoder alternately makes and breaks when the encoder is rotated, and this switching action triggers delayed pulse generator IV.G-11 via encoder driver IV.G-10. The output of the delayed pulse generator triggers one-shot IV.G-9-21, provided that no inhibit is present. (This inhibit brackets the arithmetic cycle and prevents an encoder read-in during the cycle time). The output of the one-shot loads the doppler command from the encoder into a shift register (IV.G-4, 5, 6 and 7) via a set of BIM 2's (IV.G-1, 2 and 3). The data in this shift register are shifted to the adder (via matrix IV.H-10-21) during the arithmetic cycle, and also recirculated back into the register so that the command is always available.

Provision is made for manual triggering of the read-in one-shot; this is necessary since, at the beginning of an operation, the encoder might well be sitting still while the data register might contain an incorrect number.

The shaft to which the encoder is attached is geared such that one revolution equals 64 Kc.

H. Arithmetic Example (Fig. A-9)

This figure illustrates the steps involved in converting a particular input command (-285 Kc) to the form required by the synthesizer. In the example, the command sign is assumed to be minus, so the carry flip-flop is initially cleared and the command is added to the preset.

The table on the left illustrates the states assumed by the BCD-to-binary converter at each clock pulse during the arithmetic cycle, and the table on the right shows the corresponding states assumed by the arithmetic register. The right-hand columns of these tables show the command number and the preset number in binary (LSB at the top), and the two center columns show the carry and sum generated by adding these numbers.

Since the sum is shifted back into the arithmetic register, the final result is shown in the last row of the right-hand table. Immediately below this row is shown the command to the synthesizer with a "one" added at each end — these are the bits which are always present in the input to the synthesizer.

The octal input to the synthesizer is 7621 which results in an output of 14, 194, 500 cps. This is doubled and mixed with 15. 104 Mc to give the final desired output of 13. 285 Mc.

I. Camp Parks Installation

The Camp Parks hardware is identical with the West Ford hardware with the following exceptions. Since there is no analog computer at Camp Parks, the analog input logic (Fig. A-7) is not included: the console control switch (Fig. A-1) is wired so that the analog select level to IV. H-4-24 (Fig. A-3) and to IV. H-10-26 (Fig. A-6) is always at -5 v, and the digital select level to IV. H-10-27 (Fig. A-6) is always at + 5 v.

Also, since there is no intersite coupling at Camp Parks, the input to IV. H-10-8 is tied to -5 v (Fig. A-6).

J. Layout (Figs. A-8 and A-10)

The card layout of the equipment is shown in Fig. A-8. All cards are standard, with the exception of binary-to-octal converter cards which are shown on Fig. A-10.

TABLE I

COMMAND	STAGE 4	STAGE 3	STAGE 2	STAGE 1
0	0	0	0	0
1	128000	16000	2000	250
2	256000	32000	4000	500
3	384000	48000	6000	750
4	512000	64000	8000	1000
5	640000	80000	10000	1250
6	768000	96000	12000	1500
7	896000	112000	14000	1750

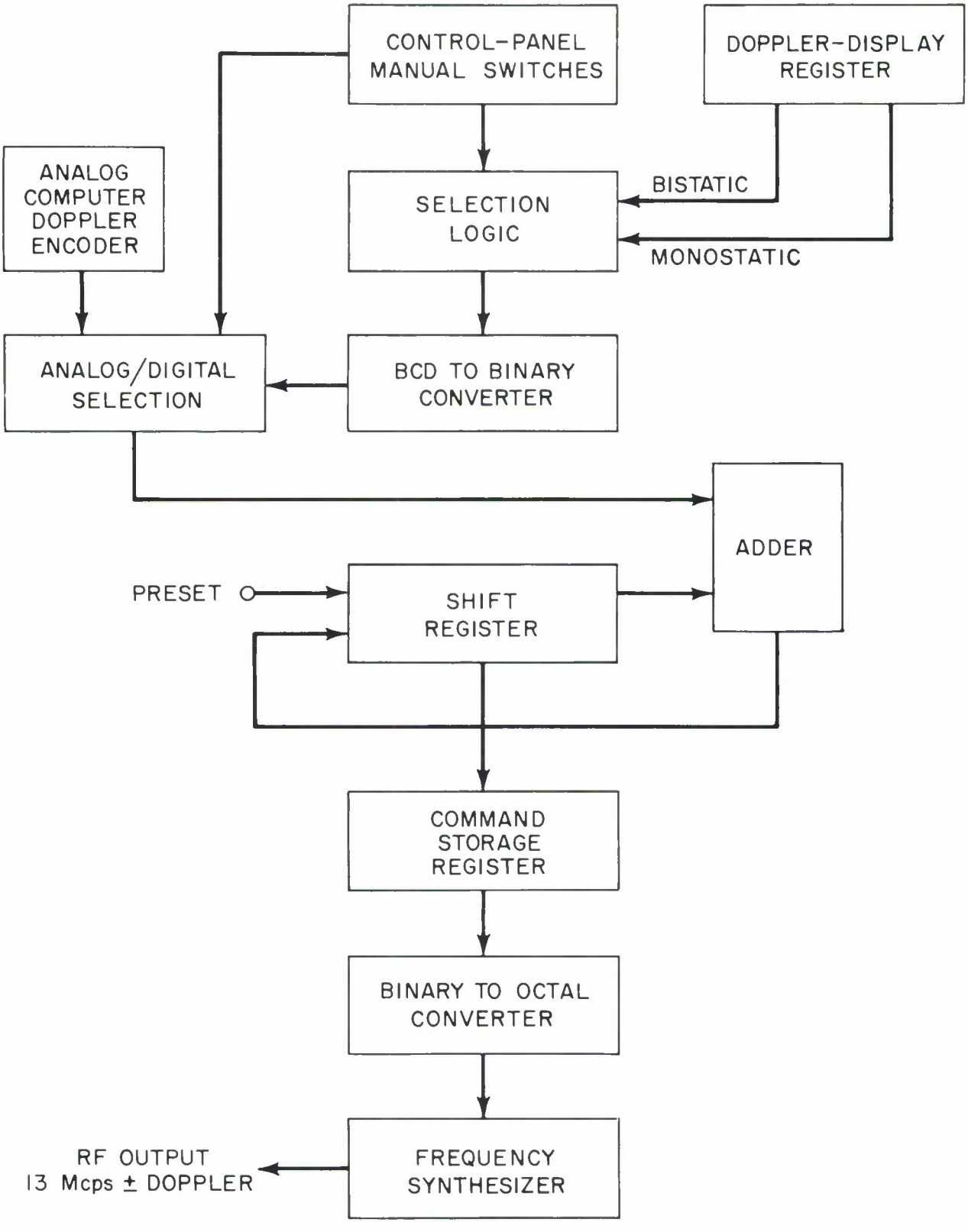

Fig. 1. Automatic doppler control system.

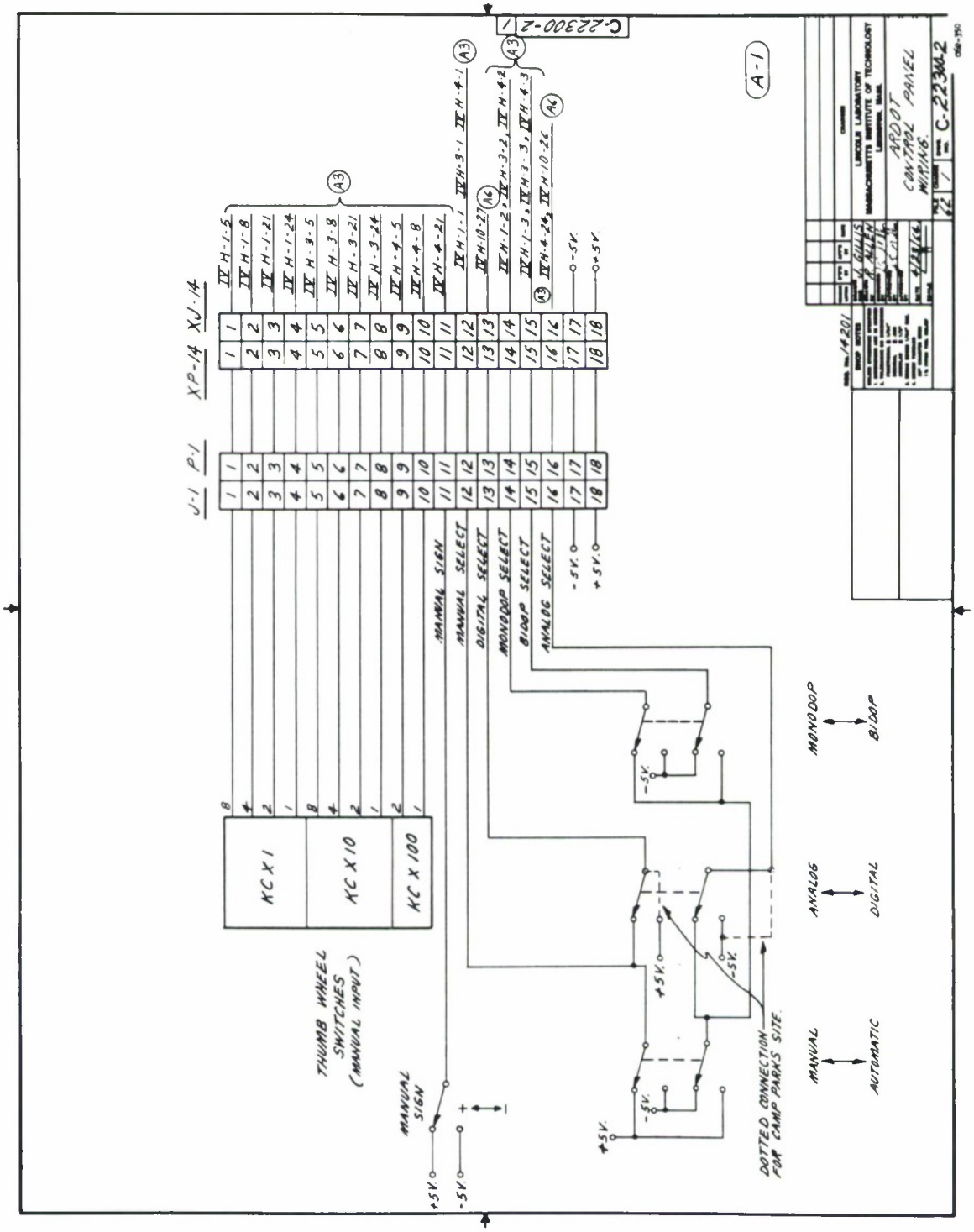

Fig. A-1. Ardot control panel wiring.

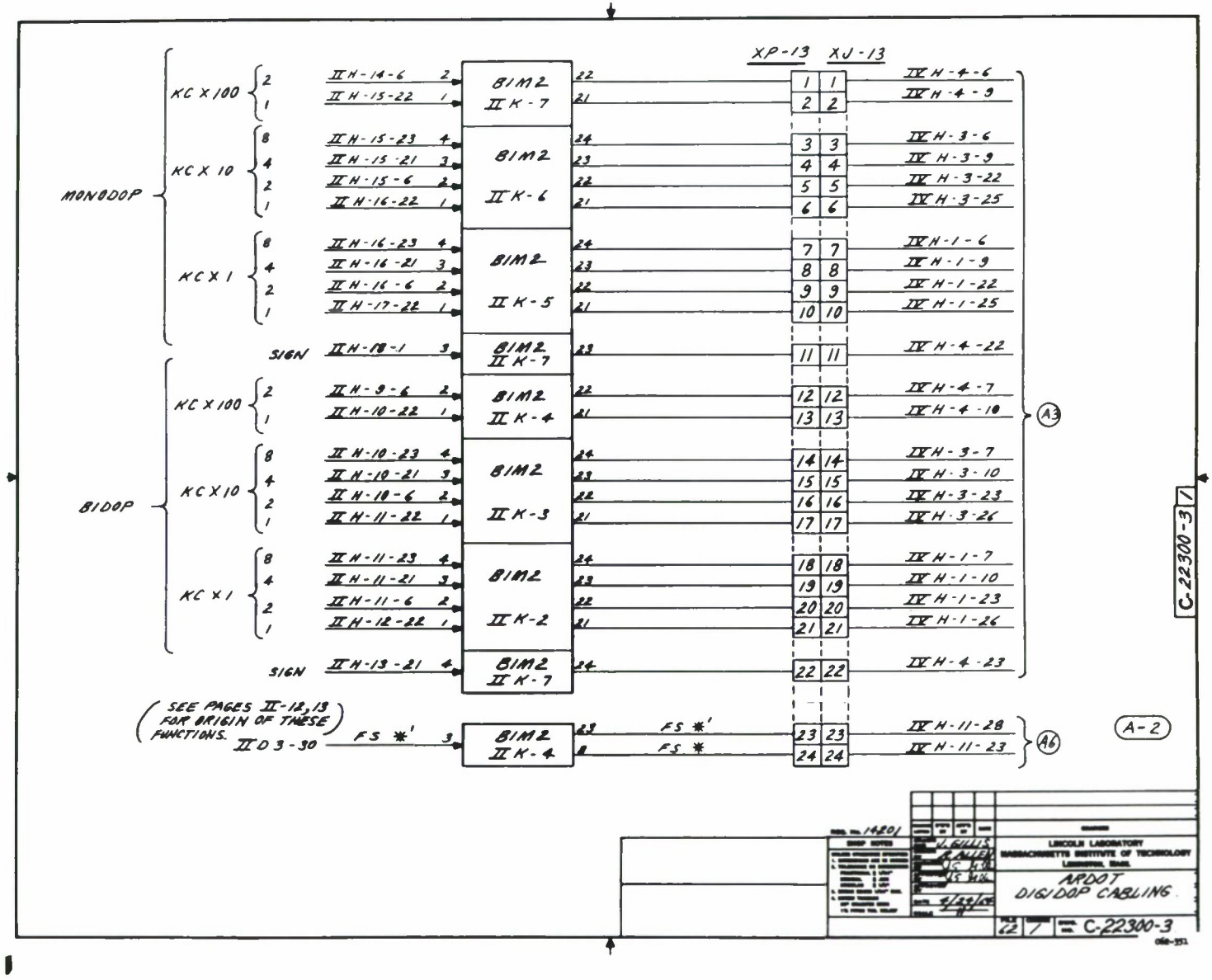

Fig. A-2. Ardot digidop cabling.

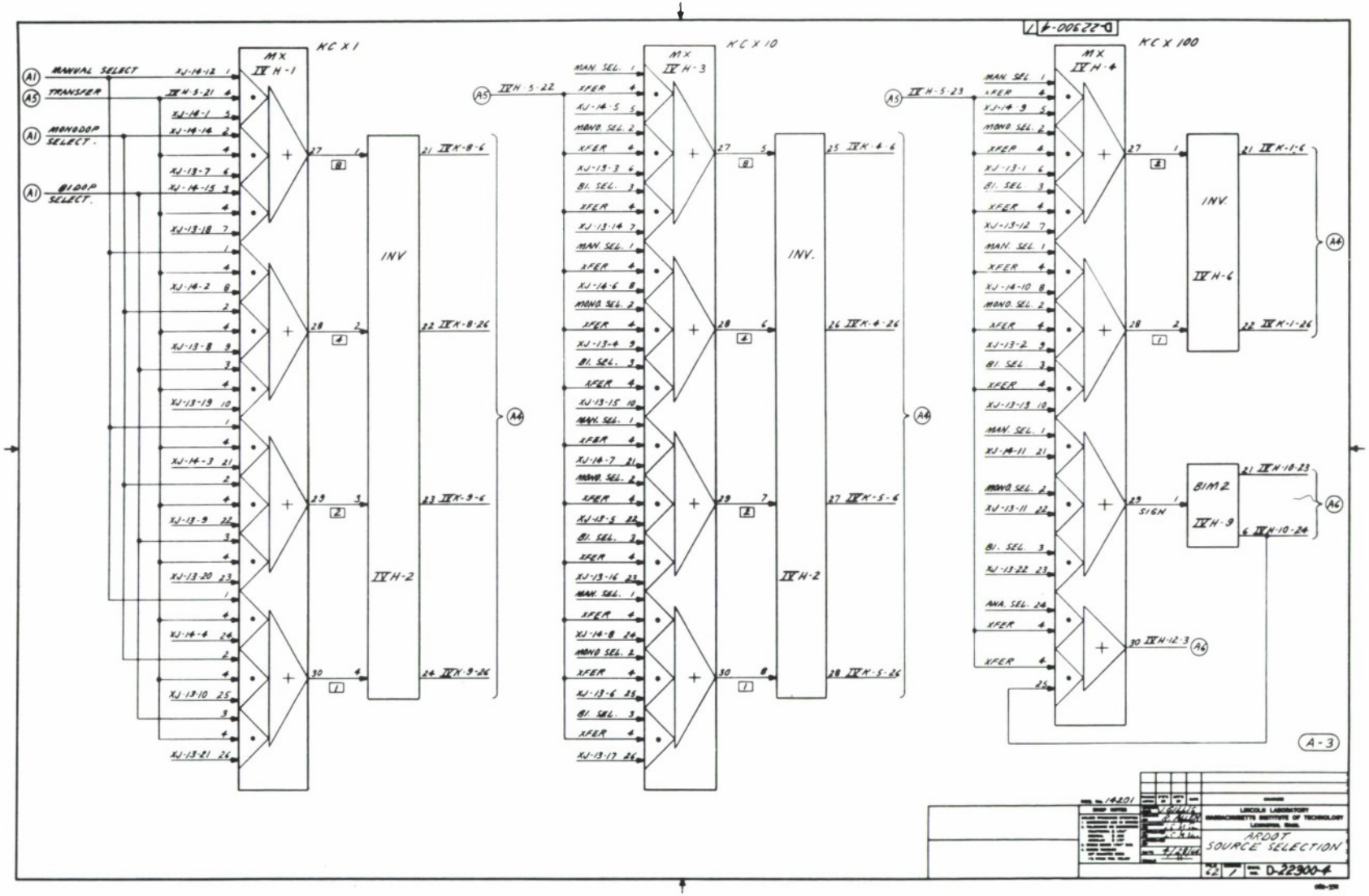

Fig. A-3. Ardot source selection.

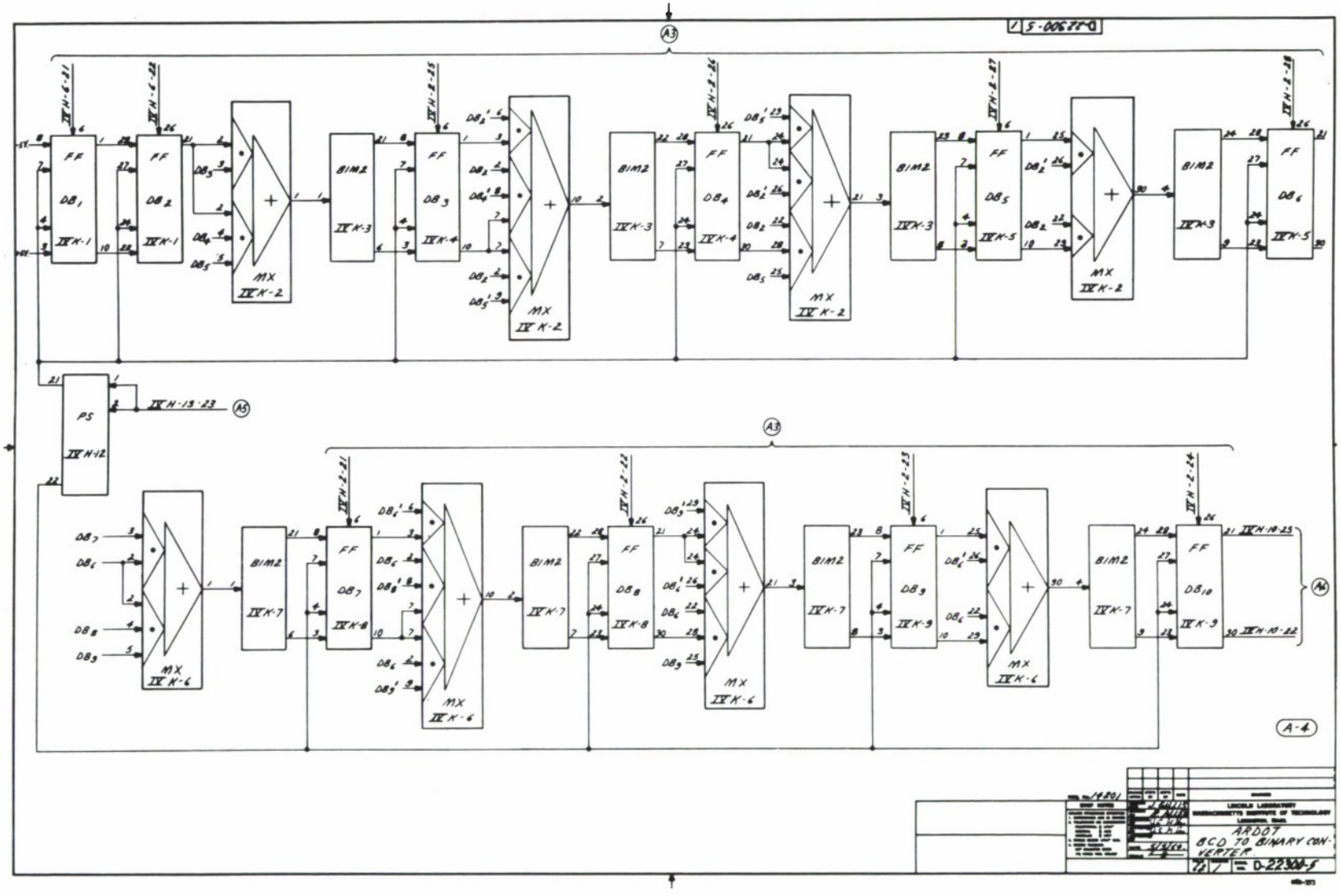

Fig. A-4. Ardot BCD-to-binary converter.

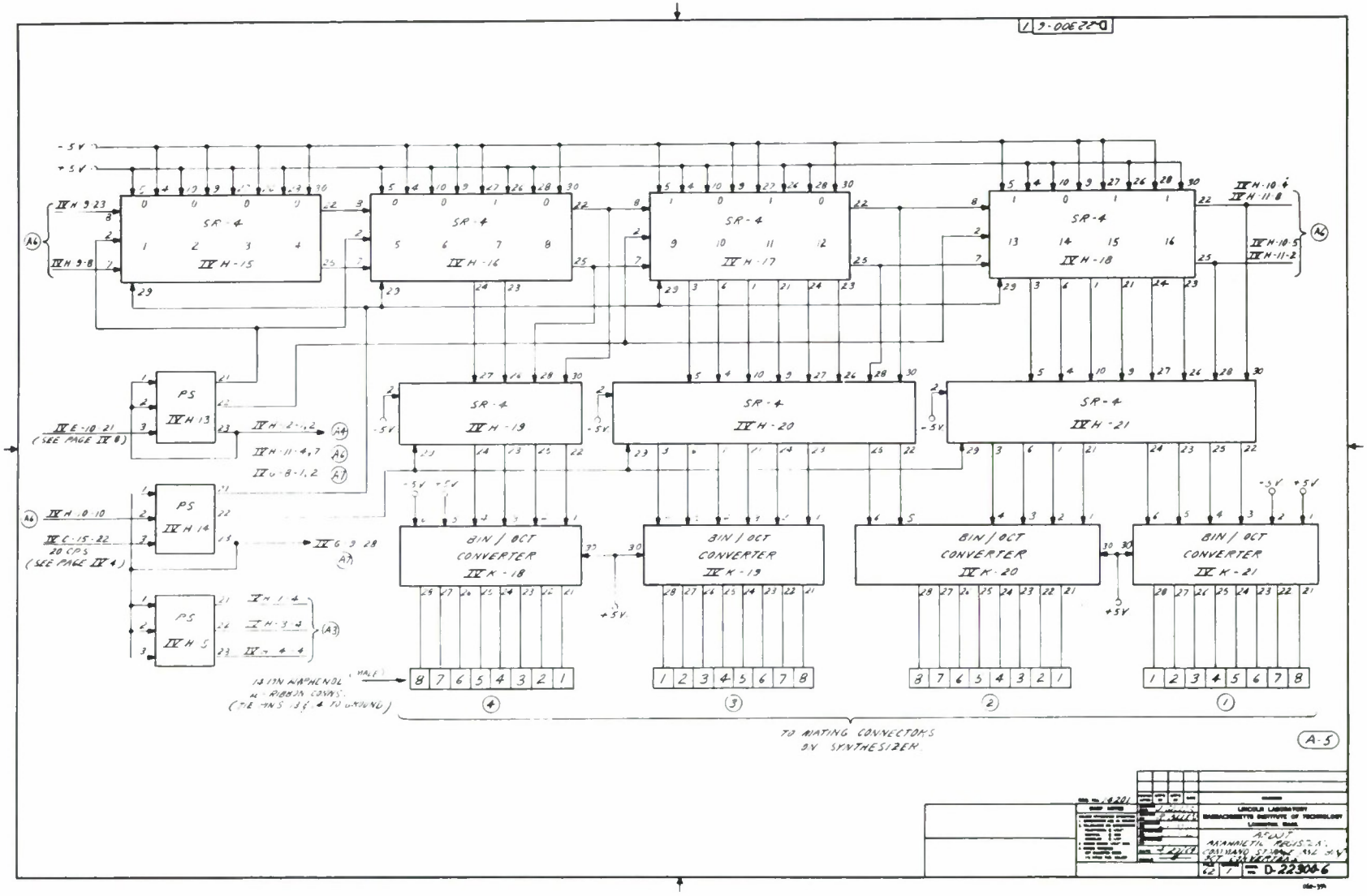

Fig. A-5. Ardot arahmetic register, command storage and bin/oct converters.

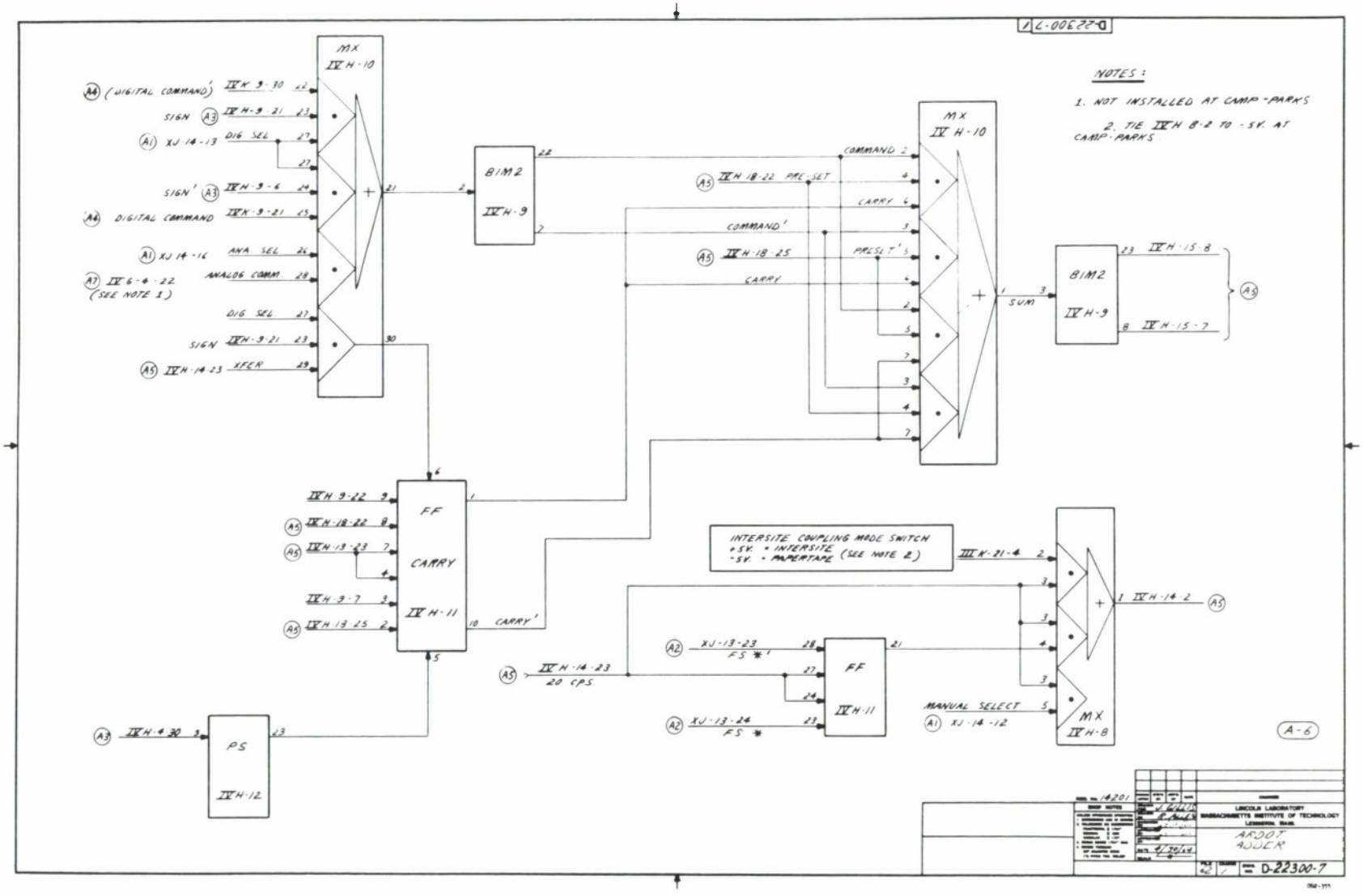

Fig. A-6. Ardot adder.

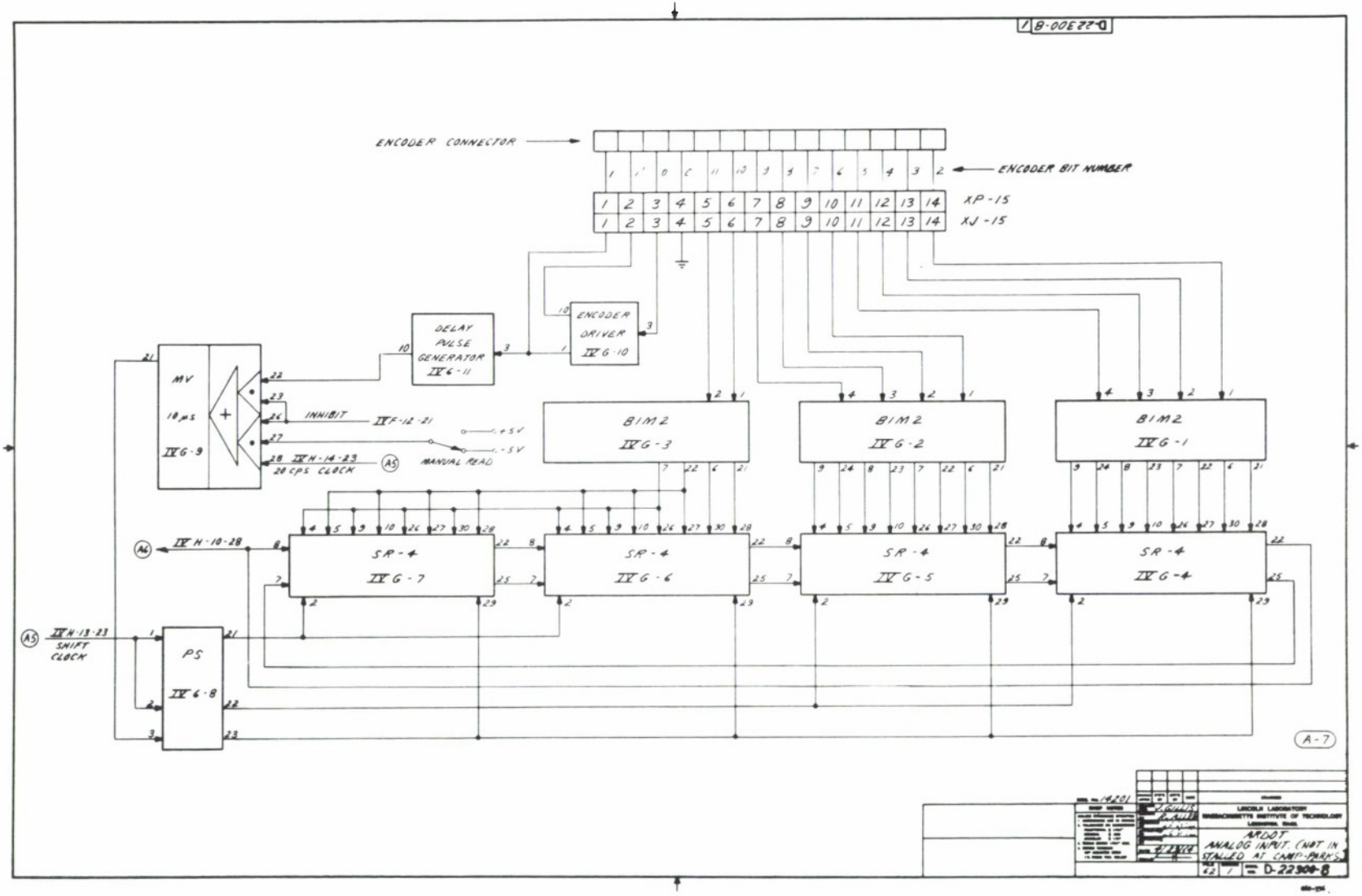

Fig. A-7. Ardot analog input. (Not installed at Camp Parks.)

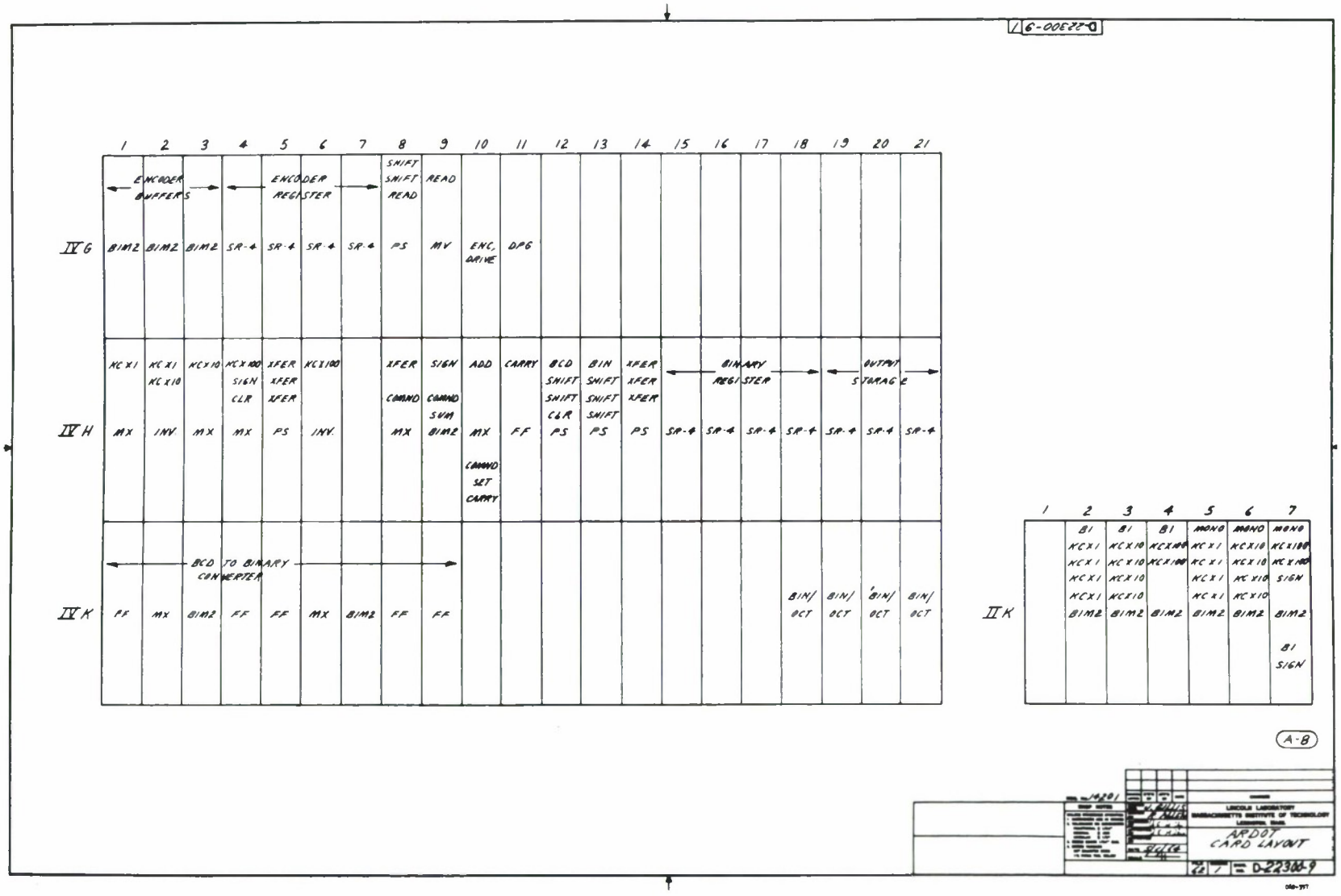

Fig. A-8. Ardot card layout.

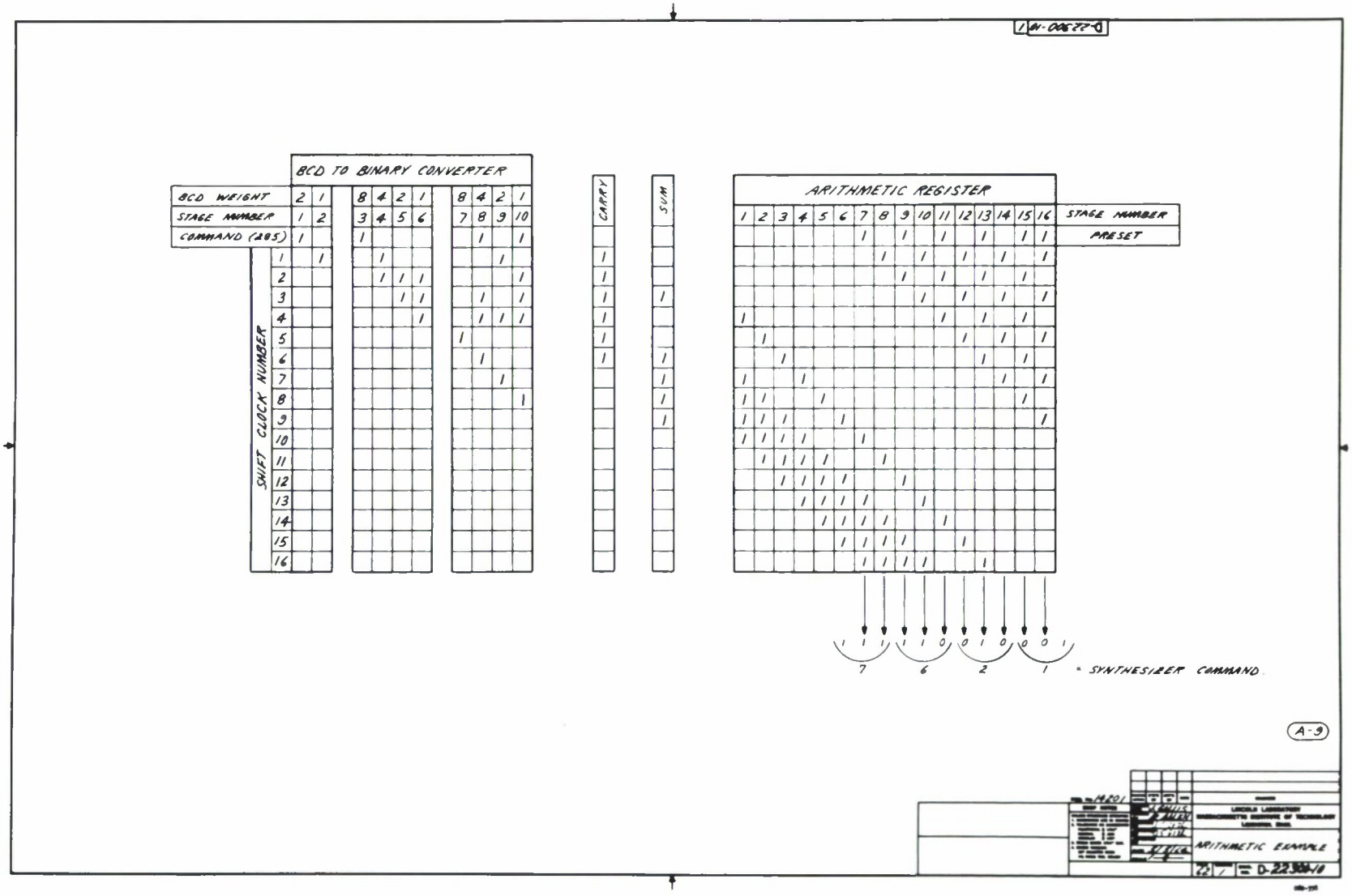

Fig. A-9. Arithmetic example.

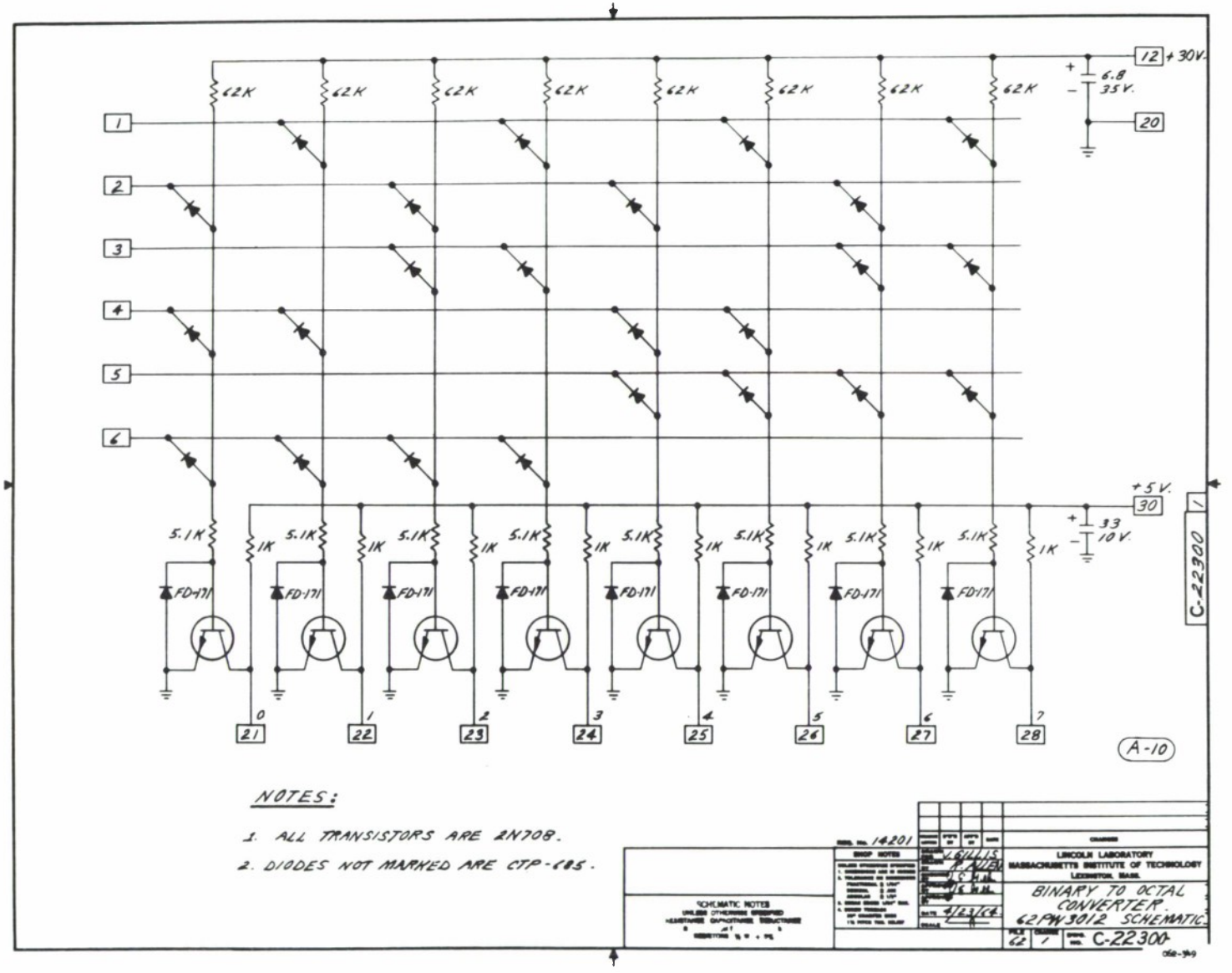

Fig. A-10. Binary-to-octal converter.

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